REMARKS

In the First Office Action, the Examiner noted that claims 1-36 are pending in the application, and that claims 1-36 are rejected. By this response, claims 1, 11, 20, and 29 are amended. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

Rejection of Claims Under 35 U.S.C. §103

The Examiner rejected claims 1-36 as being unpatentable over Pham et al. (U.S. Patent 6,212,593, issued April 3, 2001) ("Pham"). The rejection is respectfully traversed.

More specifically, the Examiner stated that Pham teaches a streaming interface configured to transmit and receive a communication sequence to and from a device configured for direct access to memory circuitry. (Office Action, p. 2). The Examiner also stated that Pham discloses control logic for implementing a plurality of DMA engines and a set of registers configured to store control data for the DMA engines. (Office Action, p. 2). The Examiner conceded that Pham does not explicitly disclose transmitting and receiving a communication sequence, but that Pham teaches a DMA unit with substantially identical function/operation. The Examiner concluded that it would have been obvious to modify Pham to transmit and receive such a communication sequence. (Office Action, p. 3-4).

Pham generally teaches a microcontroller having an execution unit, system peripherals, memory peripherals, and serial communication peripherals coupled to an internal system bus. (Pham, col. 2, lines 15-20; FIG. 1A). The serial communication peripherals include a universal serial bus (USB) and a high-level data link controller (HDLC). (Pham, col. 2, lines 16-60). Pham discloses that HDLC channels and the USB controller can be written to and read from by a DMA unit that provides for chained buffers accessed via pairs of DMA channels. (Pham, col. 2, lines 62-65).

Pham, however, does not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, Pham does not teach or suggest "a

and from said device," as recited in Applicants' claim 1. A "streaming interface" is a non-shared interface, in contrast with a bus, which is a shared interface. (See Applicants' specification, paragraphs 0044 and 0045). To clarify the invention, Applicants' have amended claim 1 to recite that the streaming interface is a non-shared interface to the memory circuitry.

In Pham, the serial communication peripherals, including the USB controller and the HDLC controller, are coupled to an internal bus. The USB and HDLC controllers of Pham must utilize the internal bus to communicate with the memory peripherals. There is not teaching or suggestion in Pham that any of the serial communication peripherals, including the USB and HDLC controllers, facilitate communication between a device and memory or the memory peripherals using a non-shared interface. As such, the USB controller and HDLC controller in Pham are not streaming interfaces, as defined in Applicants' claim 1. That is, the USB and HDLC controllers of Pham do not teach or suggest non-shared interfaces to memory circuitry. Furthermore, Pham is based on a bus architecture and there is no suggestion or motivation to modify Pham to employ a streaming interface, as recited in Applicants' claim 1. Accordingly, Pham does not render obvious Applicants' invention recited in claim 1.

Independent claims 11, 20, and 29, as amended, recite features similar to those in claim 1 emphasized above. Since Pham does not teach or suggest communication using a streaming interface as recited in claim 1, Pham also fails to render obvious claims 11, 20, and 29. Finally, claims 2-10, 12-19, 21-28, and 30-36 depend either directly or indirectly from claims 1, 11, 20, or 29. Since Pham does not render obvious claims 1, 11, 20, and 29, Pham does not render obvious claims 2-10, 12-19, 21-28, and 30-36.

Therefore, Applicants contend that claims 1-36 are patentable over Pham and, as such, fully satisfy the requirements of 35 U.S.C. §103. Accordingly, Applicants respectfully request that the present rejection of such claims be withdrawn.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims he is requested to contact Michael R. Hardaway at (408) 879-6149 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 22, 2006.

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